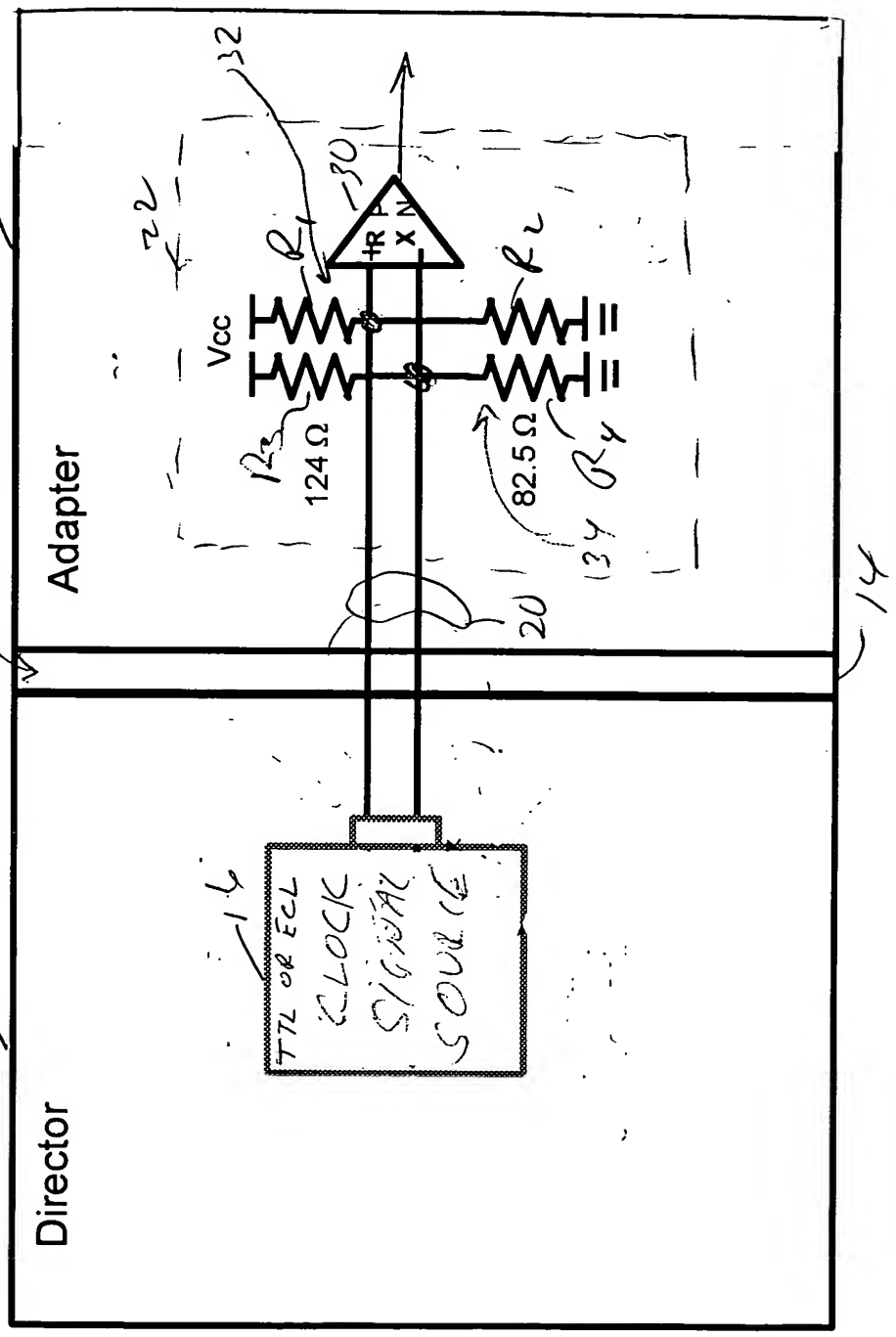

Adapter
Director
BACKPLANE
12
22
32
30
R1
R2
Vcc
124 Ω
82.5 Ω
R4
34
20
14
16
TTL OR ECL
CLOCK
SIGNAL
SOURCE

FIG 1

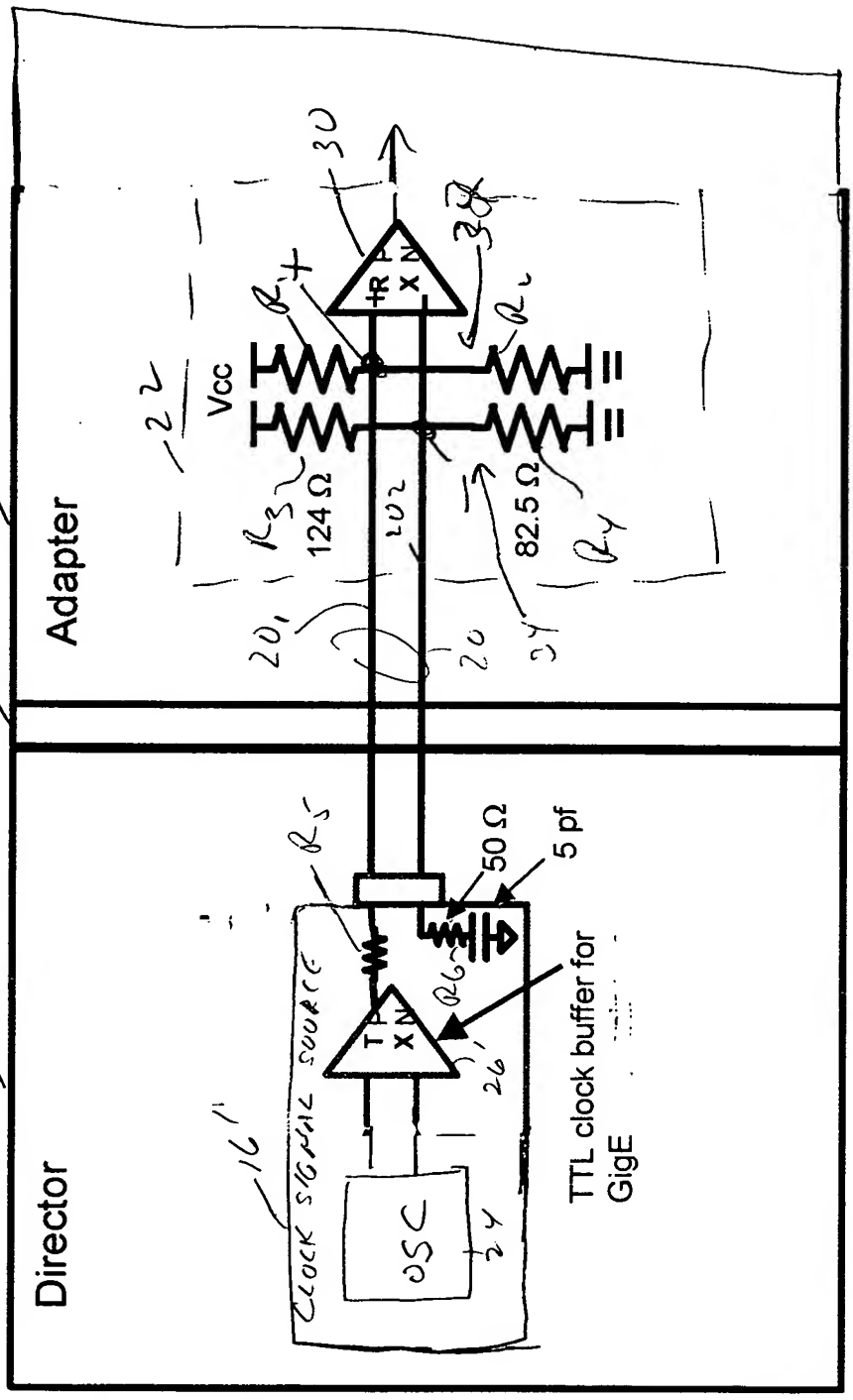
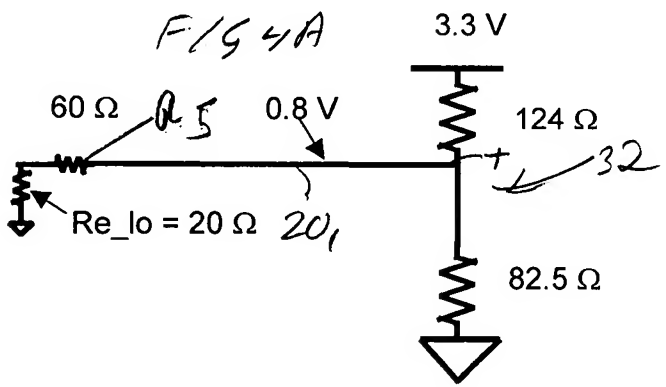
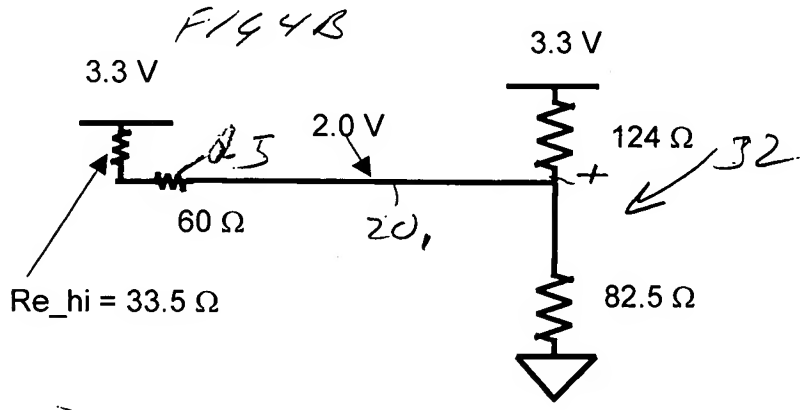

Adapter
Director
Vcc
124 Ω
82.5 Ω
50 Ω
5 pf
TTL clock buffer for
GigE
OSC

Fig 2

Equivalent DC circuit of TTL clock





TTL output low

TTL output high

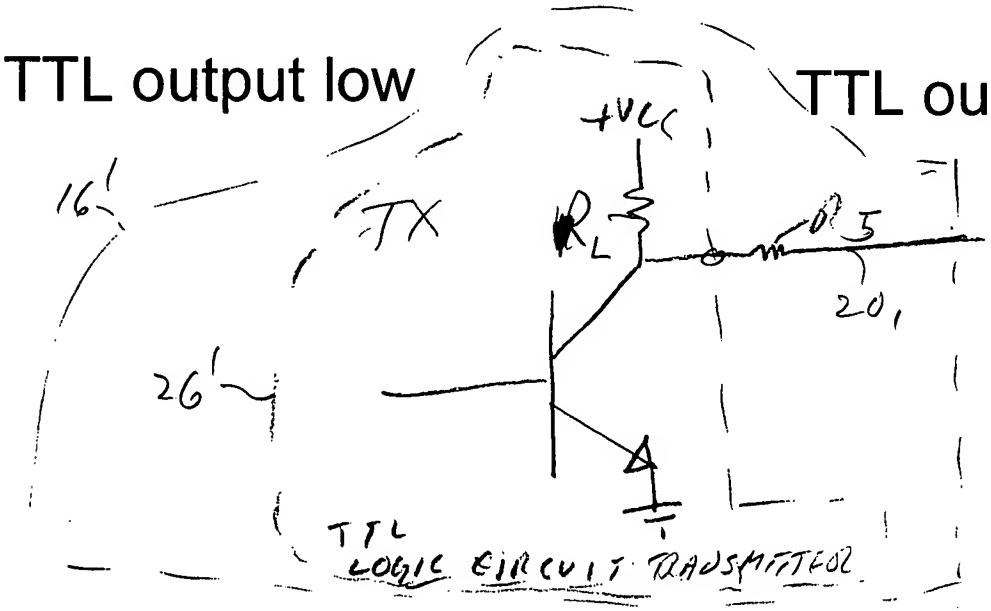


FIG 3

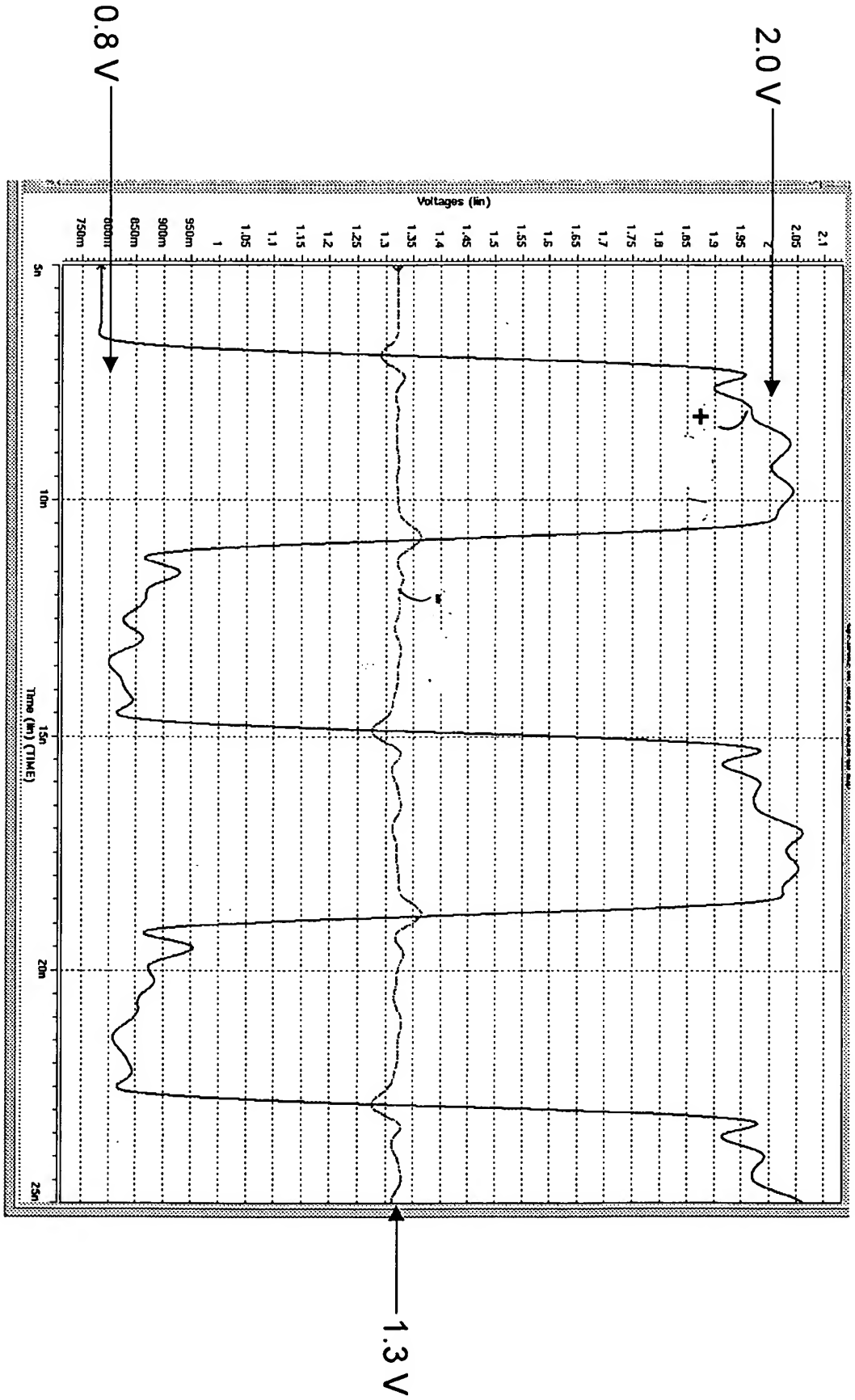
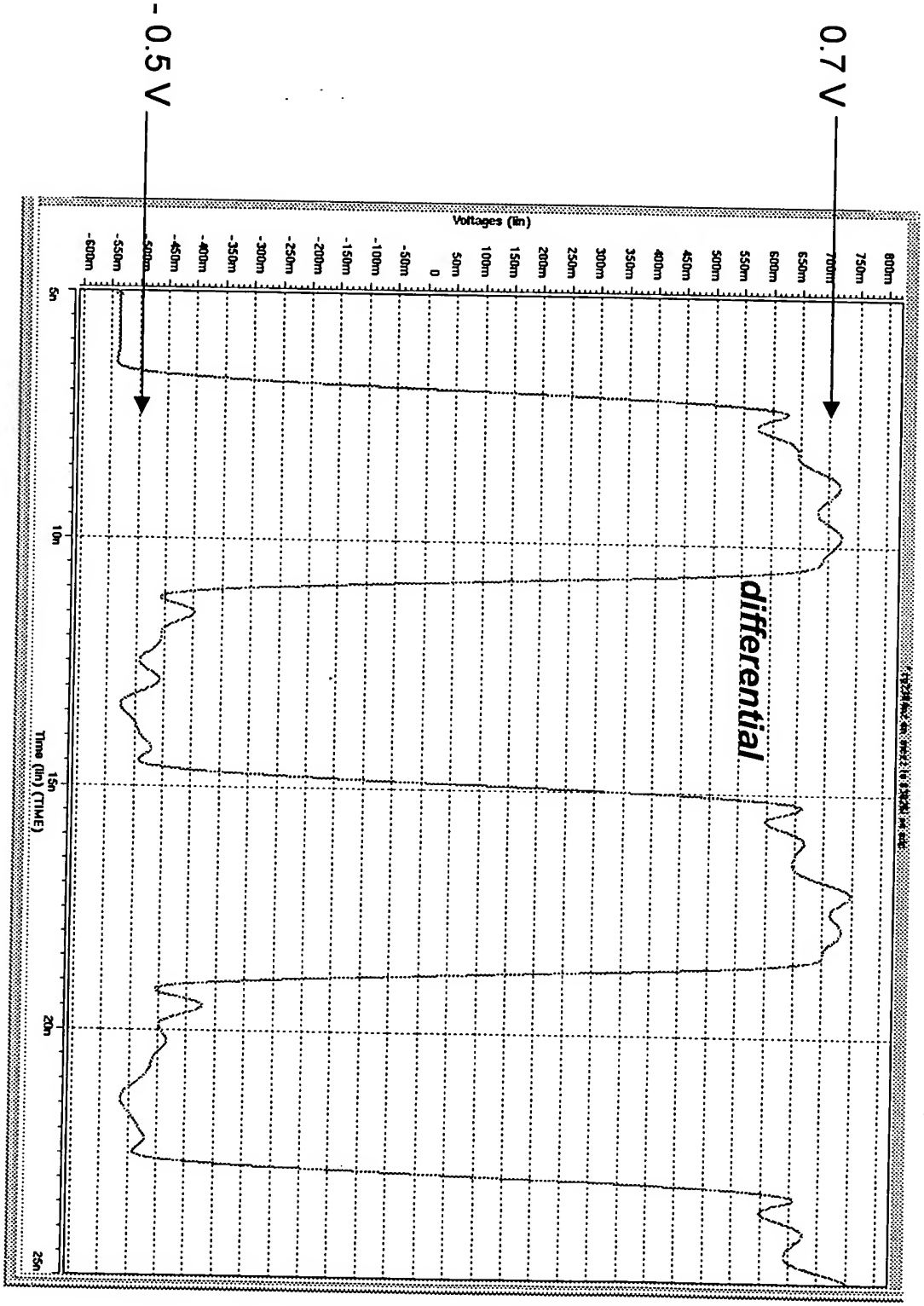

TTL clock inputs (+ and – of RX)
2.0 V
0.8 V
1.3 V
Voltages (lin)
Time (lin) (TIME)

Fig. 5



TTL clock inputs ('+' – '–' of RX)

Fig 6.

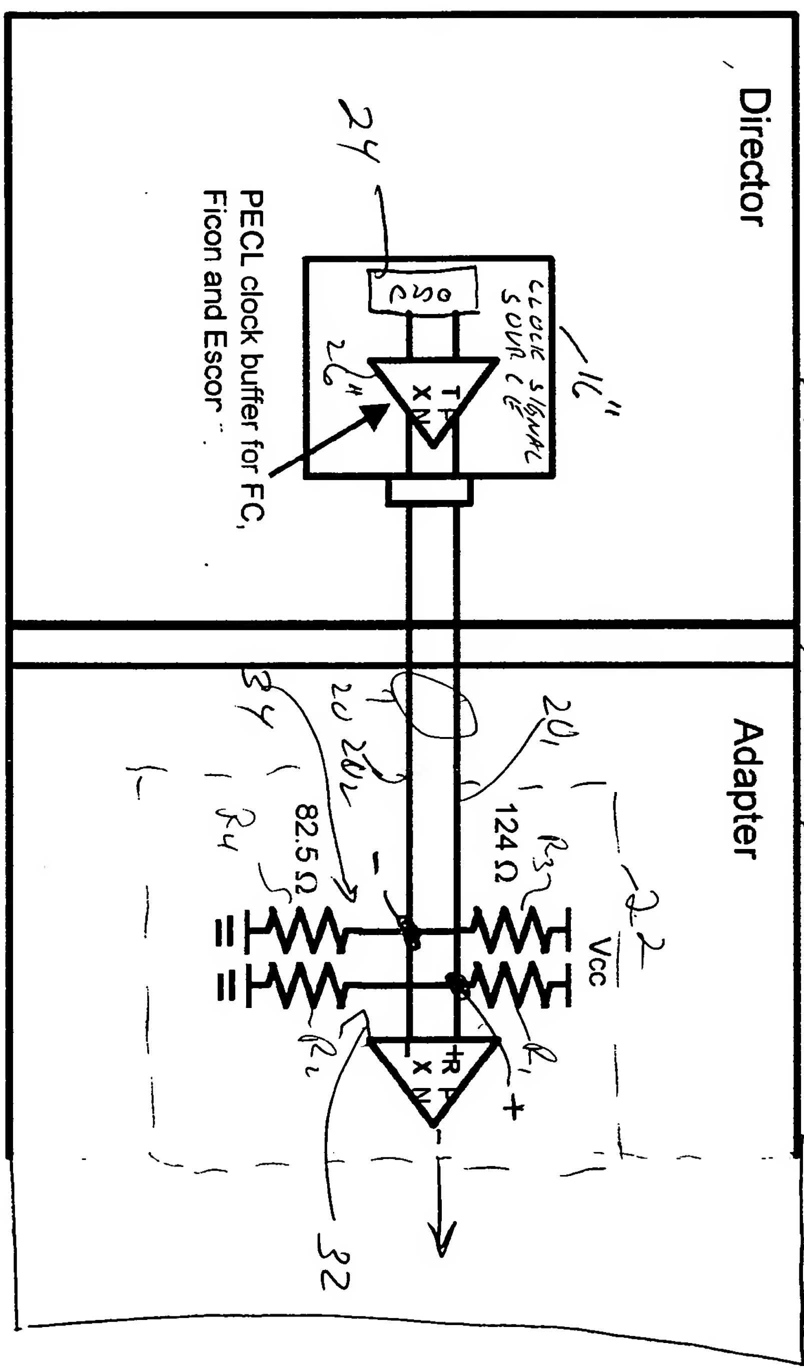

Director
Adapter
PECL clock buffer for FC, Ficon and Escon
TX
RX
124 Ω
82.5 Ω
Vcc
OSC
CLOCK SIGNAL SOURCE

FIG. 7

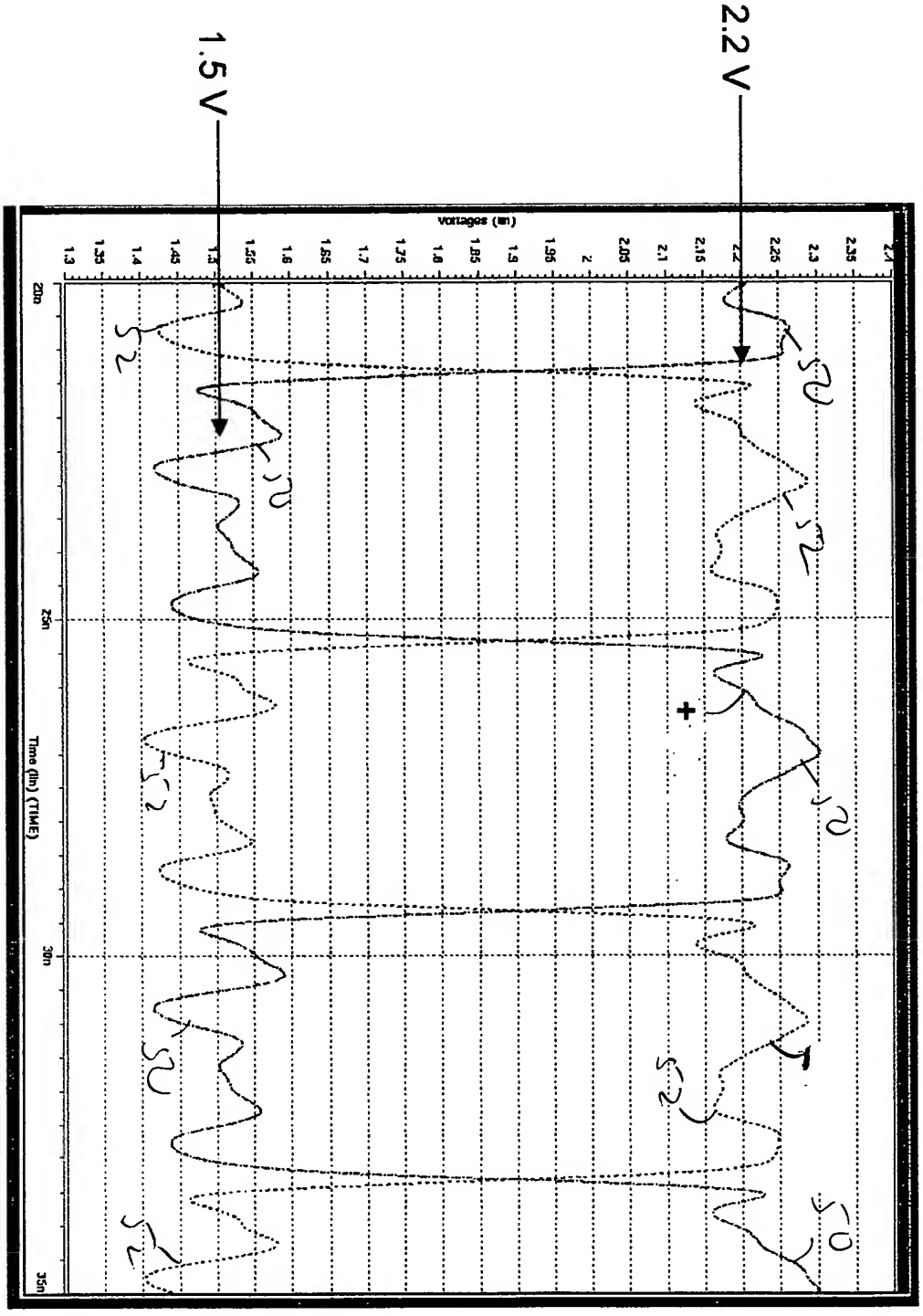

PECL clock input signals (+ and – of RX)
2.2 V
1.5 V
Voltages (m)
Time (lin) (TIME)
20n
25n
30n
35n

Fig. 8

PECL clock input signals ('+' – '–' side)

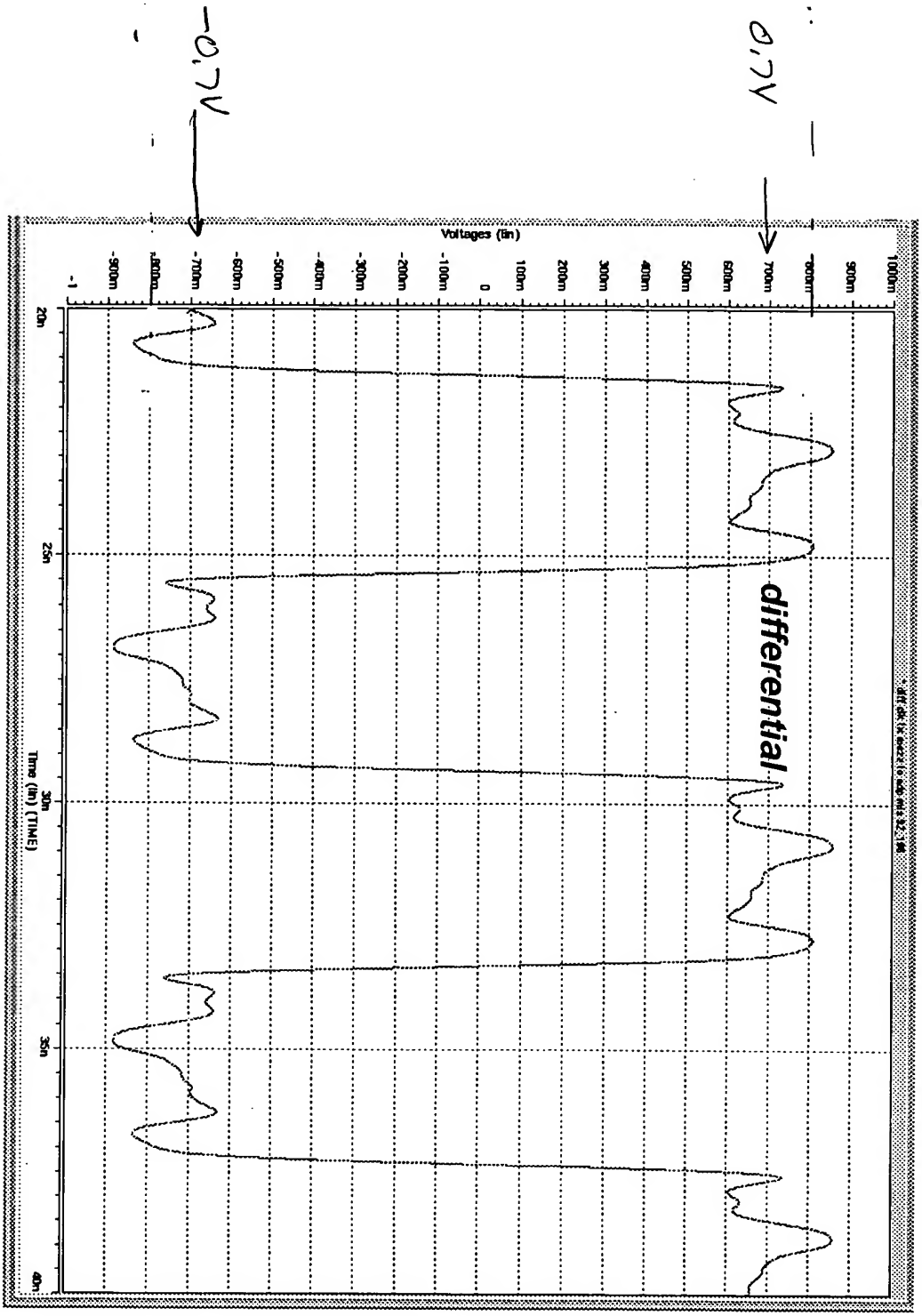


Fig 9